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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,410	02/04/2002	Christopher W. Hill	3380.1US (97-842.1)	8302

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,410	HILL ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicants' RCE filing request is acknowledged.

2. Claims 1-28 are pending in the application.

Response to Amendment

3. The amendment filed 1/2/2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "without reacting material of the at least one exposed, doped area."

In fact, the only paragraph [0028] relating to the aforementioned limitation in the original specification states "[s]ince **minimal amounts** of the semiconductor substrate 106 are consumed by these reactions ..." (Emphasis added) Since the at least one exposed, doped area 107 actually is in the semiconductor substrate 106 (i.e. silicon or polysilicon), as the selective silicide contact 108 is formed, at least a **minimal amount of the semiconductor substrate 106 is consumed, including** the at least one exposed, doped area 107. Thus, the newly added limitation **"without** reacting material of the at least one exposed, doped area" is **not** supported by the originally filed specification. (Emphasis added)

Accordingly, the aforementioned limitation will **not** be treated in its merit in this Office Action. Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 8-13, 15-17, 20 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US 3,801,365) in view of Levine et al. (US 5,989,999).

In re claim 1, Hrzek, in Fig. 3 and related text, teaches the claimed method for fabricating an interconnect adjacent a contact of a semiconductor device structure, comprising:

- causing a chemical reaction adjacent to a surface of at least one exposed, doped ares 74 of the semiconductor device structure (col. 6, lines 44-51; col. 7, lines 10-14) to selectively deposit metal silicide 78 thereon without substantially depositing metal silicide 78 onto locations 73 of the semiconductor device structure that are laterally adjacent said at least one exposed, doped area 74; and
- depositing an interconnect material 80 or 80/86/82 onto said metal silicide 78.

In re claims 20, 27 and 28, Hrzek also teaches the claimed method for fabricating a selective contact and a local interconnect on a semiconductor device structure, comprising:

- causing a chemical reaction adjacent to an exposed active device region 74 of the semiconductor device structure (col. 6, lines 44-51; col. 7, lines 10-14) to selectively deposit a contact material 78 (i.e. metal silicide) thereon without substantially depositing the contact material 78 onto a region 73 of the semiconductor device structure that are laterally adjacent said exposed active device region 74; and

- depositing an interconnect material 80 or 80/86/82 onto said contact material 78.

In contrast, Hrzek is silent as to depositing the interconnect material *in situ* with said depositing said contact material or said metal silicide.

However, Levine et al., in an analogous art, teach utilizing *in situ* deposition technique for forming said metal silicide for the purposes of reducing contaminations and manufacturing units. (col.3, lines 39-48)

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to employ said in situ deposition technique as taught by Levine et al. for depositing the interconnect material of Hrzek in situ with depositing said contact material or said metal silicide of Hrzek, since by this manner it would minimize undesirable contaminations and reduce manufacturing costs. (col.3, lines 39-48, Levine et al.).

In re claim 8, Hrzek in view of Levine et al. teaches the claimed method, as stated above, including said metal silicide comprising titanium silicide, wherein Hrzek further teaches utilizing titanium tetrachloride or titanium tetrabromide as metallic precursor for depositing said titanium silicide. (col.10, lines 19-20, 52-58, Hrzek)

In re claims 9 and 25, Hrzek in view of Levine et al. teaches the claimed method, as stated above, including that depositing said interconnect material 80 or 80/86/82 comprises blanket depositing said interconnect material 80 or 80/86/82, i.e. depositing said interconnect material 80 or 80/86/82 on said exposed, doped area 74 and said adjacent region 73. (Fig.3, Hrzek)

In re claims 10 and 26, Hrzek in view of Levine et al. teaches the claimed method, as stated above, further comprising patterning said interconnect material 80 over said contact material 78 as shown in Fig.3 in Hrzek.

In re claims 11 and 24, Hrzek teaches selectively depositing metal silicide 78 onto the exposed area 74 and depositing the interconnect material 80 onto the metal silicide 78 as shown in Fig.3. Hrzek further indicates that when the exposed area is as deep as the depth of 64 (Fig.2), more silicide layers can be selectively depositing onto the exposed area 64, as the silicide layer 68 has not reached the edge of the exposed area 64.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to further selectively deposit said interconnect material 80 after selectively depositing said metal silicide 78, in light of the teaching shown in Fig.2, since by doing so it would eliminate a step of patterning said interconnect material, which, in turn, would simplify manufacturing processing.

In re claims 12, 13 and 23, Hrzek in view of Levine et al. also teaches depositing a layer 82/86 of electrically conductive material (i.e. Al and Mo) over said interconnect material 80 (Fig.3, Hrzek); and further patterning said layer 82/86 as the same manner as patterning a layer 102 using a photoresist layer (Fig.4 and col. 14, lines 19-23).

In re claims 15 and 17, Hrzek in view of Levine et al. further teaches depositing said metal silicide (i.e. molybdenum silicide) comprising reacting a metallic precursor (i.e. such as molybdenum pentacholoride; col.8, lines 64-67, Hrzek) with a silicon-containing compound (i.e. SiCl4, col.9, line 21, Hrzek).

In re claim 16, Hrzek in view of Levine et al. also teaches the claimed method, as stated above, further comprising reacting a metallic precursor comprising the titanium tetrahalide (i.e. titanium tetrachloride; col.10, lines 19-20, 52-58, Hrzek) if the metal silicide is the titanium silicide.

6. Claims 2-5, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US '365) in view of Levine et al. (US '999) as applied to claims 1, 8-13, 15-17, 20 and 23-28 above, and further in view of Chang et al. (US 5,043,299).

In re claims 2-4 and 21, Hrzek in view of Levine et al. teaches the claimed method, as stated above, but fails to teach exposing said at least one exposed, doped area of the semiconductor device structure to a plasma comprising an activated species of at least one of nitrogen, hydrogen, and ammonia; and cleaning the semiconductor device structure.

Chang et al., in an analogous art of selective deposition, teach a pre-deposition preparation by exposing the exposed, doped area of the semiconductor device structure to plasma comprising an activated species of at least one of nitrogen and hydrogen (Fig.1 and text in col. 3, lines 14-26; col. 4, lines 10-15); and cleaning the semiconductor device structure (col.7, lines 1-11) for the purpose of removing contaminants including undesirable oxide and moisture (col.2, lines 15-28; col.6, lines 48-61).

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to expose the exposed, doped area of semiconductor device structure of Hrzek in view of Levine et al. by the plasma comprising either nitrogen or hydrogen and cleaning the semiconductor device structure, as taught by Chang et al., since by doing so it would be beneficial to the subsequent selective deposition.' (col.2, lines 15-28; col.6, lines 48-61, Chang et al)

In re claim 5, Hrzek in view of Levine et al. and further in view of Chang et al. further teach that said cleaning includes employing a cleaning agent comprising chlorine. Particularly,

Chang et al. indicate using a halogen-containing gas, which at least would include chlorine and fluorine, for the cleaning purpose. (col.7, lines 5-6).

In re claim 22, Hrzek in view of Levine et al. and further in view of Chang et al. do not teach exposing the semiconductor device structure to a nitrogen-ammonia plasma. However, the selection of the cleaning plasma for said exposing step is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the cleaning plasma can be selected for the particular surface to be cleaned, dependent upon the material of the particular surface. (col.3, lines 14-26, Chang et al.) In this case, the applicant is required to demonstrate the criticality, generally by showing that the claimed plasma would achieve unexpected results relative to the prior art. See M.P.E.P. 2144.05 III.

7. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US '365) in view of Levine et al. (US '999) as applied to claims 1, 8-13, 15-17, 20 and 23-28 above, and further in view of Kolar et al. (US 5,162,259).

Hrzek in view of Levine et al. teaches the claimed method, as stated above, but fails to teach cleaning the semiconductor device structure after said depositing said metal silicide, wherein said cleaning includes employing a cleaning agent comprising at least one of chlorine, hydrochloric acid, and hydrofluoric acid.

Kolar et al. in an analogous art teach forming a silicide layer 40 followed by cleaning the semiconductor device structure employing a cleaning agent comprising hydrochloric acid, prior to depositing an interconnect material 38. (Fig.4 and text in col. 21-23)

Therefore, one of the ordinary skill in the art, at the time the invention was made, would have been motivated to utilize said hydrochloric acid as cleaning agent as taught by Kolar et al., in the method of Hrzek in view of Levine et al to clean the surface of said deposited metal silicide and then to deposit said interconnect material, since by doing so it would improve the adhesion between adjacent layers.

8. Claims 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hrzek (US '365) in view of Levine et al. (US '999) as applied to claim 1 above, and further in view of Park et al. (US 6,087,257).

In re claim 14, Hrzek in view of Levine et al. teaches the claimed method but fails to teach that depositing said interconnect material comprises depositing at least one of titanium and titanium nitride.

However, Park et al. in an analogous art teach forming a titanium silicide 14 onto an exposed, doped area 12 of a semiconductor substrate 10; depositing said titanium nitride 15; and depositing an electrically conductive layer 16 onto said titanium nitride 15,wherein said titanium nitride 15 acts as a diffusion barrier layer (Fig.1E and text in col.1, lines 50-58, Park).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to deposit said titanium nitride as said interconnect material, when the underlying metal silicide is said titanium silicide as taught by Park et al., after selectively depositing said metal silicide of Hrzek; and further to proceed the deposition of said electrically

conductive layer since the selection of said interconnect material depends on the function of the device and the adjacent materials, as evidenced by Park et al. By depositing said titanium nitride as said interconnect material on said titanium silicide, prior to depositing said electrically conductive layer thereon, it would avoid diffusion problem between said titanium silicide and said electrically conductive layer. (col.1, lines 50-58, Park)

In re claims 18 and 19, Hrzek teaches the claimed method, as stated above, but fails to teach that depositing said interconnect material comprises reacting a metallic precursor with a reactant comprising at least one of ammonia, nitrogen trifluoride, an organic silane reactive gas, and an activated species; and said reacting a metallic precursor comprises at least one of a titanium tetrahalide and a Ti(NRz)4, where R is selected from the group consisting of hydrogen and alkyl groups, with said reactant.

However, Levine et al., in an analogous art of forming said titanium nitride (i.e. same material as said interconnect material in Hrzek and Park et al.), teach reacting a metallic precursor (i.e. TDMAT) with a reactant (i.e. a reactive gas), wherein said metallic precursor comprises a Ti(NRz)4, where R is selected from the group consisting of hydrogen and alkyl groups, with said reactant. (col.1, line 58 through col.2, line 13).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to deposit said interconnect material (i.e. titanium nitride) of Hrzek and Park et al. by reacting said metallic precursor with said reactant, as taught by Levine et al., since by this manner it would produce said interconnect material having satisfactory barrier function with improved resistivity. (col.3, lines 58-65, Levine et al.)

Response to Arguments

9. Applicant's arguments filed 1/2/04 have been fully considered but they are not persuasive.

Applicants argue that Hrzek does not teach or suggest the "without reacting a material", as amended. (page 7, fourth paragraph)

In response to the argument, it is submitted that the aforementioned limitation is a **new matter**, as stated above. Thus, the merit has not been treated in the Office Action. In fact, the originally filed specification **does** disclose that there is a small amount (i.e. a minimal amount) of the semiconductor substrate is reacting while selectively depositing the metal silicide.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

Feb. 6, 2004